[*METHOD OF FORMING A SYSTEM ON CHIP*]

Abstract of Disclosure

A method of forming a system on chip(SOC) comprising read only memory(ROM) and nitride read only memory(NROM) by utilizing nitride read only memory. The method is to form a plurality of field oxide layers on a surface of a substrate in order to define an active area of each device. An ONO dielectric layer is then formed on the surface of the substrate, thereafter performing a photolithography and ion implantation process to form a plurality of N-type bit lines and P-type pocket doping areas in the substrate inside the memory area. After that, an etching process is performed in order to remove regions of the ONO dielectric layer in the periphery area and regions of the ONO dielectric layer in the memory area, optionally. After that, a thermal oxidation process is utilized in order to form a buried drain oxide layer atop each bit line and a gate oxide layer on the surface of the active area in the periphery area, respectively. Then, a polysilicon layer is deposited on the surface of the substrate and a photolithography and etching process are utilized in order to simultaneously form a word line in the memory area and the gates of the periphery transistor in the periphery area. Finally, a ROM code process is performed to adjust the threshold voltage of the high threshold voltage(high Vth) device in the read only memory area.

Figures